IN THE CLAIMS

1-3. (Canceled)

4. (New) A device comprising:

a plurality of memory cells;

a controller for initiating a refresh signal;

a counter connected to the controller for receiving the refresh signal, the counter including a plurality of counter bit lines for providing a plurality of counter bits;

a plurality of storage elements including a plurality of register bit lines for providing a plurality register bits;

a plurality of compare units, each of the compare units connecting to one of the counter bit lines and to one of the register bit lines for comparing one of counter bits with one of the register bits; and

an output circuit connected to the plurality of compare units for activating a select signal based on a comparison result from each of the compare units for selectively refreshing the memory cells.

5. (New) The device of claim 4, wherein the storage elements includes a plurality of flip flops for storing the register bits representing addresses of a portion of the plurality of memory cells.

6. (New) The device of claim 6, wherein the compare units are configured for comparing the register bits with the counter bits such that only memory cells of the portion of the plurality of memory cells are refreshed when the counter bits and the register bits are matched.

7. (New) The device of claim 4, wherein each of the compare units includes a pass gate connected to one of the register bit lines and to one of the counter bit lines for passing a signal from one of the counter bit lines to the output circuit based on a signal on one of the register bit lines.

8. (New) The device of claim 7, wherein each of the storage elements includes an input node for receiving an active signal from the controller when one of the memory cells is accessed.

9. (New) The device of claim 8, wherein the output circuit includes a logic gate having input nodes connected to the compare units and an output node for providing the select signal.

10. (New) The device of claim 8, wherein the output circuit includes a multiplexer having input nodes connected to the compare units and an output node for providing the select signal.

11. (New) A device comprising:

a plurality of memory cells;

a controller connected to the memory cells;

a counter connected to the controller, the counter including a first group of counter bit lines and a second groups of counter bit lines;

a plurality of storage elements including a plurality of register bit lines;

a logic circuit connected to the storage elements for setting values in the storage elements;

a plurality of compare units, each of the compare units connecting to the second group of the counter bit lines and to one of the register bit lines; and

an output circuit connected to the compare units for activating a select signal based on signals at output nodes of the compare units to selectively refresh the memory cells.

12. (New) The device of claim 11, wherein the memory cells are located at locations corresponding to a plurality of address ranges.

13. (New) The device of claim 12, wherein each of the storage elements includes a flip flop for storing a value associated with one of the addresses ranges.

14. (New) The device of claim 13, wherein the compare units are configured for decoding signals on the second plurality of counter bit lines.

15. (New) The device of claim 11, wherein the logic circuit is configured for decoding a combination of input signals to set the values in the storage element.

16. (New) The device of claim 15, wherein the plurality of compare units includes:

a first plurality of logic gates connected to the second group of counter bit lines for decoding signals on the second plurality of counter bit lines; and

a second plurality of logic gates having input nodes connected to the first plurality of logic gates and to the register bit lines and having output nodes connected to the output nodes of the compare units.

17. (New) A device comprising:

a plurality of memory cells;

a controller connected to the memory cells;

a counter connected to the controller, the counter including a first group of counter bit lines and a second groups of counter bit lines;

a first plurality of storage elements including a first plurality of register bit lines;

a second plurality of storage elements including a second plurality of register bit lines;

a first compare circuit having input nodes and an output node, the input nodes connecting to the first group of counter bit lines and to the first plurality of register bit lines;

a second compare circuit having input nodes and an output node, the input nodes connecting to the second group of counter bit lines and to the second plurality of register bit lines; and

a select circuit having input nodes connected to the output nodes of the first and second compare circuits and having an output node for selectively activating a select signal to selectively refresh the memory cells.

18. (New) The device of claim17, wherein one of the first and second plurality of storage elements includes flip flops for storing addresses of a portion of the plurality of memory cells.

19. (New) The device of claim 17, wherein the first compare circuit includes a plurality of compare units for comparing signals on the first group of counter bit lines with signals on the first plurality of register bit lines such that only memory cells located at addresses represented by the signals on the first group of counter bit lines are refreshed when the signals on the first group of counter bit lines match the signals on the first plurality of register bit lines.

20. (New) The device of claim 19, wherein the second compare circuit includes a plurality of compare units for decoding comparing signals on the second group of counter bit lines.

21. (New) The device of claim 20, wherein the second compare circuit includes:

a first plurality of logic gates connected to the second group of counter bit lines for decoding signals on the second plurality of counter bit lines; and

a second plurality of logic gates having input nodes connected to the first plurality of logic gates and to the register bit lines and having output nodes connected to the output nodes of the compare units.

22. (New) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of memory cells;

a controller for initiating a refresh signal;

a counter connected to the controller for receiving the refresh signal, the counter including a plurality of counter bit lines for providing a plurality of counter bits;

a plurality of storage elements including a plurality of register bit lines for providing a plurality register bits;

a plurality of compare units, each of the compare units connecting to one of the counter bit lines and to one of the register bit lines for comparing one of counter bits with one of the register bits; and

an output circuit connected to the plurality of compare units for activating a select signal based on a comparison result from each of the compare units for selectively refreshing the memory cells.

23. (New) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of memory cells;

a controller connected to the memory cells;

a counter connected to the controller, the counter including a first group of counter bit lines and a second groups of counter bit lines;

a plurality of storage elements including a plurality of register bit lines;

a logic circuit connected to the storage elements for setting values in the storage elements;

a plurality of compare units, each of the compare units connecting to the second group of the counter bit lines and to one of the register bit lines; and

an output circuit connected to the compare units for activating a select signal based on signals at output nodes of the compare units to selectively refresh the memory cells.

24. (New) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of memory cells;

a controller connected to the memory cells;

a counter connected to the controller, the counter including a first group of counter bit lines and a second groups of counter bit lines;

a first plurality of storage elements including a first plurality of register bit lines;

a second plurality of storage elements including a second plurality of register bit lines;

a first compare circuit having input nodes and an output node, the input nodes connecting to the first group of counter bit lines and to the first plurality of register bit lines; and

a second compare circuit having input nodes and an output node, the input nodes connecting to the second group of counter bit lines and to the second plurality of register bit lines;

a select circuit having input nodes connected to the output nodes of the first and second compare circuits and having an output node for selectively activating a select signal to selectively refresh the memory cells.

25. (New) A method comprising:

storing addresses of a portion of a plurality of memory cells as stored addresses;

activating a refresh signal;

counting addresses of the plurality of memory cells to produce counted addresses;

comparing the counted addresses with the stored addresses; and

refreshing a memory cell within the portion of the plurality of memory cells when a counted address matches one of the stored addresses.

26. (New) The method of claim 25, wherein storing addresses occurs each time a memory cells of the plurality of memory cells is accessed.

27. (New) The method of claim 26, wherein storing addresses includes storing values in a plurality of storage elements, wherein a combination the values represents the stored addresses.

28. (New) The method of claim 27, wherein counting addresses of the plurality of memory cells includes counting row addresses of the plurality of memory cells.

29. (New) The method of claim 28, wherein the row addresses are counted sequentially.

30. (New) The method of claim 29, wherein storing addresses includes storing a value in a storage element, wherein the value in the storage element represents the stored addresses.

31. (New) The method of claim 30, wherein comparing includes decoding a portion of a plurality of counter bits, wherein a combination of the counter bits represented a counted address.

32. (New) A method comprising:

assigning a plurality of address ranges to addresses of memory cells, each of the address ranges including a number of addresses;

selecting one of the address ranges to be a selected address range;

storing the selected address range as a stored address range;

counting addresses of the memory cells during a refresh mode to produce counted addresses;

comparing the counted addresses with addresses of the stored address range; and

refreshing memory cells located at the counted addresses when the counted addresses match the addresses of the stored address range.

33. (New) The method of claim 32, wherein selecting occurs when at least one of the memory cells is accessed during a memory access mode of a memory device having the memory cells.

34. (New) The method of claim 32, wherein selecting occurs during a programming mode of memory device having the memory cells.

35. (New) The method of claim 32, wherein selecting includes applying a combination of signals to input nodes of a memory device having the memory cells, wherein the combination of signals corresponds to one of the address ranges.

36. (New) The method of claim 32, wherein storing includes storing a value in a storage element, wherein the value in the storage element represents the stored address range.

37. (New) The method of claim 36, wherein comparing includes decoding a portion of a plurality of counter bits, wherein a combination of the counter bits represented a counted address.

38. (New) A method comprising:

storing a plurality of stored bits, a combination of the stored bits corresponding to a number of addresses of a number of memory cells;

activating a refresh signal;

generating a plurality of counts, each of count of the counts including a number of count bits, wherein a combination of the count bits represents an address of a memory cell;

comparing the number of count bits of each of the counts with the plurality of stored bits; and

omitting a refresh of memory cells located at addresses represented by the number of count bits when the number of count bits and the plurality of stored bits are mismatched.

39. (New) The method of claim 38, wherein storing a plurality of stored bits includes storing each of the stored bits in one storage element of a register.

40. (New) The method of claim 38, wherein the number of count bits includes a first count bits and a last count bit, wherein the plurality of stored bits includes a first stored bit and a last stored bit, and wherein comparing includes:

comparing the first count bit with the first stored bit; and

comparing the last count bit with the last stored bit.

CONCLUSION

Claims 1-3 are canceled and claims 4-40 are added; claims 4-40 are now pending in this application.

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully Submitted,

SCOTT J. DERNER ET AL.

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